Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method of fabricating an integrated circuit, comprising the following steps, performed in order:

providing a semiconductor body having a top metal interconnect level formed thereon, said top metal interconnect level having a first and a second metal interconnect line;

depositing a material over said top metal interconnect level;

patterning and etching said material to form a bottom electrode on said first metal interconnect line and a cladding on said second metal interconnect line;

forming a capacitor dielectric ~~layer~~ over said bottom electrode; ~~and~~

forming a top electrode ~~layer~~ over said capacitor dielectric;

forming a protective overcoat over said top electrode and said top metal interconnect level; and

forming a conductive cap partially over said protective overcoat, said conductive cap electrically connecting said top electrode and said second metal interconnect line.

2. (Cancelled)

3. (original) The method of claim 1, further comprising the steps of patterning and etching said capacitor dielectric layer and said top electrode layer to form a capacitor dielectric and top electrode, wherein said cladding protects said second metal interconnect line during said etching.

4. (original) The method of claim 1, wherein said material and said top electrode layer each comprise TaN.

5. (original) The method of claim 1, wherein said material and said top electrode layer each comprise one or more layers of material selected from the group consisting of TaN, TiN, Ru, Ir, and Ta.

6. (original) The method of claim 1, wherein said capacitor dielectric layer comprises tantalum-oxide.

7. (original) The method of claim 1, wherein said capacitor dielectric layer comprises hafnium-oxide or silicon nitride.

8. (original) The method of claim 1, wherein said first and second metal interconnect lines comprise copper.

9. (Currently amended) An integrated circuit comprising:

a topmost metal interconnect level located over a semiconductor body, said topmost metal interconnect level comprising a first and a second metal interconnect line;

a decoupling capacitor located over said topmost metal interconnect level, wherein a bottom electrode of said decoupling capacitor is electrically connected to said first metal interconnect line;

a cladding on said second metal interconnect line, wherein said cladding and said bottom electrode comprise the same material; and

an aluminum cap layer electrically connecting a top electrode of said decoupling capacitor to said second <u>metal</u> ~~copper~~ interconnect line.

10. (cancelled).

11. (original) The integrated circuit of claim 9, wherein said cladding and said bottom electrode comprise TaN.

12. (original) The integrated circuit of claim 9, wherein said cladding and said bottom electrode each comprise one or more layers of material selected from the group consisting of TaN, TiN, Ir, Ru, and Ta.

13. (original) The integrated circuit of claim 9, wherein said capacitor dielectric comprises tantalum-oxide.

14. (original) The integrated circuit of claim 9, wherein said capacitor dielectric comprises hafnium-oxide or silicon nitride.

15. (original) The integrated circuit of claim 9, wherein said first and second metal interconnect lines comprise copper.